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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,922	07/08/2004	Jung-Pill Kim	082123-0310458	8429

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EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,922	KIM, JUNG-PILL	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed September 13, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *19-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated September 13, 2005, claims 1-23 are active in this application.

Claim Objections

2. Claims 19-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-6 are rejected under 35 U.S.C 102(b) as being anticipated by Mueller et

al. [U.S. Patent #6,320,780].

With respect to claim 1, Mueller et al. disclose, in column 1, lines 45-60 and column 2, lines 1-15, a method of data access, said method comprising: precharging a first bit line and a second bit line ["...bitline pair is selected after the bitlines are precharged..."]; permitting charge sharing between a capacitance of a memory cell and one of the precharged first bit line and the precharged second bit line ["...coupling the memory cell's capacitor to the bitline true..."]; biasing the other of the precharged first bit line and the precharged second bit line ["...reference bitline increases or decreases along with the voltage swing on the bitline true..."]; and subsequent to said permitting charge sharing and said biasing, sensing a difference between a potential of the first bit line and a potential of the biased second bit line ["...a sense amplifier coupled to the bitline pair senses and amplifies the differential voltage signal..."].

With respect to claim 2, Mueller et al. disclose, in column 2, lines 1-15, that the biasing includes altering a potential of the second bit line ["...reference bitline increases or decreases along with the voltage swing on the bitline true..."].

With respect to claim 3, Mueller et al. disclose, in column 2, lines 1-15, that the biasing includes reducing a potential of the second bit line ["...reference bitline increases or decreases along with the voltage swing on the bitline true..."].

With respect to claim 4, Mueller et al. disclose, in column 1, lines 45-60, that the sensing a difference between a potential of the first bit line and a potential of the second bit line includes amplifying said difference ["...a sense amplifier coupled to the bitline pair senses and amplifies the differential voltage signal..."].

With respect to claim 5, Mueller et al. disclose, in column 1, that the permitting charge sharing includes applying a potential to a gate of a transistor of the memory cell. It is noted that the memory cell being referred to has a transistor [see column 1, lines 15-20]. The gate is being connected to a word line [see column 1, line 20]. It is well known in the art that in order to select a particular cell, the word line connected to that particular cell would have to be selected. In order to select that particular word line, a potential would need to be placed on that particular word line. Hence, by applying a potential to that particular word line, that potential would be applied to the gate of that particular transistor.

With respect to claim 6, Mueller et al. disclose, in column 1, that the biasing includes applying a potential to a bias capacitor coupled to the second bitline. It is noted that the memory cell being referred to has a transistor and a capacitor [see column 1, lines 15-20]. The gate is being connected to a word line [see column 1, line 20]. It is well known in the art that in order to select a particular cell, the word line connected to that particular cell would have to be selected. In order to select that particular word line, a potential would need to be placed on that particular word line. Hence, by applying a potential to that particular word line, that potential would be applied indirectly to the capacitor of the cell by way of the transistor.

5. Claims 7-10 are rejected under 35 U.S.C 102(b) as being anticipated by Yamada et al. [U.S. Patent #5,375,095].

With respect to claim 7, Yamada et al. disclose, in figures 1a, 1b, 6a and 6b, a method of data access, said method comprising: selecting a wordline ["...word lines 3 is then selected..." – see column 10, lines 55-60]; asserting a bias signal corresponding to the word line ["...whereby that word line rises to the high level potential..." – see column 10, lines 55-60]; and sensing the difference between a potential of a bitline coupled to the word line and a potential of a reference bit line ["...that potential difference is then amplified by the sense amplifier circuit..." – see column 10, lines 60-65. It is also noted that the bitlines are coupled to the wordlines via cell – see figures 1a and 1b.], wherein charge sharing between a memory cell and the bit line coupled to the word line occurs as a consequence of said selecting a word line ["...whereby that word line rises to the high level potential. As a result, the charge that is held in a corresponding one of the memory cells that is coupled to the bit line pair ... is transferred to one of these bit lines..." – see column 10, lines 55-65], and wherein the potential of the reference bit line is altered as a consequence of said asserting a bias signal [..."causing a minute potential difference to be produced between these bit lines..." – see column 10, lines 55-65.].

With respect to claim 8, Yamada et al. disclose, in column 10, lines 50-60, that the asserting a bias signal occurs subsequent to said selecting a word line ["...whereby the word line rises to the high level potential..."].

With respect to claim 9, Yamada et al. disclose, in column 10, lines 50-60, that the sensing a difference includes sensing a difference between the potential of the bitline and the altered potential of the reference bit line ["...that potential difference is

then amplified by the sense amplifier..." – it is noted that the sense amplifier has to sense the potential first before it can amplify that particular potential.].

With respect to claim 10, Yamada et al. disclose, in column 4 and figure 3, that the potential of the reference bit line is reduced as a consequence of said asserting a bias signal. A2, of figure 3, indicates that the voltage of the bitline drops after the selection of the word line.

6. Claims 11-13 are rejected under 35 U.S.C 102(b) as being anticipated by Mueller et al. [U.S. Patent #6,320,780].

With respect to claim 11, Mueller et al. disclose, in column 1, lines 45-60 and column 2, lines 1-15, a method of data access, said method comprising: precharging a first bit line and a second bit line ["...bitline pair is selected after the bitlines are precharged..."]; permitting charge sharing between a capacitance of a memory cell and the precharged first bit line ["...coupling the memory cell's capacitor to the bitline true..."]; biasing a selected one of the precharged bit lines ["...reference bitline increases or decreases along with the voltage swing on the bitline true..."]; and subsequent to said permitting charge sharing and said biasing, sensing a difference between a potential of the first bit line and a potential of the biased second bit line ["...a sense amplifier coupled to the bitline pair senses and amplifies the differential voltage signal..."].

With respect to claim 12, Mueller et al. disclose, in column 2, lines 1-15, that the biasing includes altering a potential of the selected bit line ["...reference bitline increases or decreases along with the voltage swing on the bitline true..."].

With respect to claim 13, Mueller et al. disclose, in column 2, lines 1-15, that the biasing includes applying a potential to a bias capacitor coupled to the selected bit line ["...reference bitline increases or decreases along with the voltage swing on the bitline true..." – it is noted that the capacitor is connected to the bitline pair via cell transistor].

7. Claims 14-18 are rejected under 35 U.S.C 102(b) as being anticipated by Kumanoya et al. [U.S. Patent #4,933,907].

With respect to claim 14, Kumanoya et al. disclose a semiconductor memory device comprising: a precharging circuit [4 of figure 13a is shown as being an inherent feature within the art] configured and arranged to precharge a bitline and a reference bitline [BL and /BL]; a memory cell [MC of figure 13a is shown as being an inherent feature within the art] configured and arranged to share charge with the bit line [this happens with a respected word line of an MC gets selected and the stored charge within the MC gets transferred to the bitline]; a bias circuit [110 via 13 of figure 1] configured and arranged to bias a potential of the reference bit line to increase a refresh period in a semiconductor memory device [see column 18, lines 10-25 – as noted in the cited section, element 110 alters the timing of a refreshing operation]; and a sense amplifier [12] configured and arranged to sense a difference between a potential of the bitline and a potential of the reference bitline.

With respect to claim 15, Kumanoya et al. disclose, in figure 13a, that it is well known to have a field-effect transistor [Qo] and a capacitor [Co] within a memory cell [MC].

With respect to claim 16, Kumanoya et al. disclose, in figure 13a, that the memory cell [MC] is coupled to a wordline [WL] and is further configured and arranged to share charge with the bitline upon a predetermined alteration in a potential of the wordline. As noted in the earlier rejections, the charge stored within a memory cell is transferred to the bitline upon the selection of a particular wordline. It is noted that a potential would be place on that particular word line upon the selection of it.

With respect to claim 17, Kumanoya et al. disclose that the bias circuit is configured and arranged to reduce a potential of the reference bitline. It is noted that if a particular element is not selected, it's potential would be changed to zero; hence, the potential of that particular element is reduced.

With respect to claim 18, Kumanoya et al. disclose a bias circuit, as stated above. It is noted that all electrical elements have parasitic components such as capacitance.

Allowable Subject Matter

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- The bias capacitor includes a metal-oxide-semiconductor field effect transistor having a low threshold voltage.
- The bias capacitor includes an n-channel metal oxide semiconductor field effect transistor having a low threshold voltage.
- A second memory cell configured and arranged to share charge with the bitline; a first isolation circuit configured and arranged to isolate the memory cell from the sense amplifier; and a second isolation circuit configured and arranged to isolate the second memory cell from the sense amplifier.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
November 18, 2005

MICHAEL TRAN
PRIMARY EXAMINER